1. (currently amended) Method for forming a highly relaxed semiconductor layer ~~(52; 63.1; 74)~~ with a thickness between 100nm and 800nm in a growth chamber ~~(23)~~ with gas inlet ~~(26, 30)~~, comprising the steps:
   - providing a substrate ~~(25; 51; 61; 71)~~ in the growth chamber ~~(23)~~ on a substrate carrier,
   - maintaining a constant substrate temperature ($T_S$) of the substrate ~~(25; 51; 61; 71)~~ in a range between $350^0$C and $500^0$C,
   - establishing a high-density, low-energy plasma in the growth chamber ~~(23)~~ such that the substrate ~~(25; 51; 61; 71)~~ is being exposed to the plasma,
   - directing Silane gas ($SiH_4$) and Germane gas ($GeH_4$) through the gas inlet ~~(26, 30)~~ into the growth chamber ~~(23)~~, the flow rates of the Silane gas and the Germane gas being adjusted in order to form said semiconductor layer ~~(52; 63.1; 74)~~ by means of low-energy plasma enhanced chemical vapor deposition with a growth rate in a range between 1 and 10 nm/s, said semiconductor layer ~~(52; 63.1; 74)~~ having a Germanium concentration x in a range between $0 < x < 50\%$.

2. (currently amended) The method of claim 1, whereby the forming of the semiconductor layer ~~(52; 63.1; 74)~~ takes less than 5 minutes, preferably between 1 and 4 minutes.

3. (currently amended) The method of claim 1, whereby the substrate temperature ($T_S$) is maintained constant during the formation of the semiconductor layer ~~(52; 63.1; 74)~~, the substrate temperature ($T_S$) preferably having a fluctuation of ± 5%.

4. (original) The method of claim 1, whereby the substrate is a <100> or <111> oriented silicon wafer or a Silicon-on-Insulator (SOI) substrate.

5. (currently amended) The method of claim 1 ~~one of the preceding claims~~, whereby the substrate has a potential of about – 12 Volts and the plasma potential is close to 0 Volts.

6. (currently amended) The method of claim 1 ~~one of the preceding claims~~, whereby a thin silicon buffer layer ~~(62)~~ is formed on the substrate ~~(61)~~ prior to the forming of the semiconductor layer ~~(63.1)~~, said thin silicon buffer layer ~~(62)~~ preferably being formed at a substrate temperature in a range between $700^0$C and $750^0$C.

7. (currently amended) The method of claim 1 ~~or 6~~, whereby the uppermost part of the substrate ~~(25; 51)~~ is treated by means of a dry-etching or wet-etching step prior to the forming of the semiconductor layer ~~(51; 63.1)~~.

8. (original) The method of claim 1, whereby the substrate temperature is in a range between $380^0$C and $420^0$C.

9. (original) The method of claim 1, whereby the growth rate is in a range between 1.5 nm/s and 4 nm/s.

10. (currently amended) The method of claim 1, whereby the semiconductor layer ~~(52; 63.1; 74)~~ after completion of the deposition has a thickness in a range between 100nm and 800nm.

11. (currently amended) The method of claim 1 ~~one of the preceding claims~~, whereby the semiconductor layer ~~(52; 63.1; 74)~~ shows a self-relaxation during the formation so that the semiconductor layer ~~(52; 63.1; 74)~~ after completion of the formation has a relaxation of more than 75%.

12. (currently amended) The method of claim 1 ~~one of the preceding claims~~, whereby the semiconductor layer ~~(52; 63.1; 74)~~ after completion of the formation has a surface roughness (rms) of less than 1.8nm and/or a peak-to-valley height difference of less than 5nm.

13. (currently amended) The method of claim 1, whereby a further step is carried out after the forming of the semiconductor layer ~~(63.1)~~, during said further step a second semiconductor layer ~~(63.2)~~ being formed having a Germanium concentration in a range between $50 < x < 100\%$, said second semiconductor layer ~~(63.2)~~ being formed at a second substrate temperature.

14. (original) The method of claim 13, whereby the second substrate temperature ($T_{S2}$) is in a range between the substrate temperature ($T_S$) used during the forming of the semiconductor layer and the substrate temperature ($T_S$) minus $50^0$C.

15. (original) The method of claim 1, whereby said growth chamber is a high-density, low-energy plasma enhanced chemical vapor deposition (LEPECVD) chamber.

16. (original) The method of claim 1, whereby an annealing step is carried out after completion of the forming of the semiconductor layer, said annealing step preferably being carried out at a temperature in a range between $600^0$C and $870^0$C.

17. (original) The method of claim 1, whereby a total reactive gas flow at the gas inlet is chosen between 5 sccm and 50 sccm.

18. (currently amended) Heterostructure semiconductor device ~~(50; 60; 80)~~, comprising a substrate ~~(25; 51; 61; 71)~~, a highly relaxed epitaxial $Si_{1-x}Ge_x$ layer

~~(52; 63.1; 74)~~ with constant concentration x of Ge, an active region ~~(59; 70; 76)~~ being situated above said $Si_{1-x}Ge_x$ layer ~~(52; 63.1; 74)~~, said highly relaxed $Si_{1-x}Ge_x$ layer ~~(52; 63.1; 74)~~ having a thickness between 100nm and 800nm and a degree of relaxation of at least 75%.

19. (currently amended) The device of claim 18, whereby said $Si_{1-x}Ge_x$ layer ~~(52; 63.1; 74)~~ has a surface roughness (rms) of less than 1.8nm and/or a peak-to-valley height difference of less than 5nm.

20. (currently amended) The device of claim 18, whereby the substrate ~~(51; 61; 71)~~ is a <100> or <111> oriented silicon wafer or a Silicon-on-Insulator (SOI) substrate.

21. (currently amended) The device of claim 18, comprising a second semiconductor layer ~~(63.2)~~ being formed on said $Si_{1-x}Ge_x$ layer ~~(52; 63.1; 74)~~, said second semiconductor layer ~~(63.2)~~ having a Germanium concentration x in a range between $50 < x < 100\%$.

22. (original) The device of claim 20 being part of a very large scale integrated (VLSI) circuit.

23. (new) The method of claim 6, whereby the uppermost part of the substrate is treated by means of a dry-etching or wet-etching step prior to the forming of the semiconductor layer.

3 ore